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ADC WITH REDUCED QUANTIZATION NOISE AND PROGRAMMABLE BIT RESOLUTION

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CROSS REFERENCE TO RELATED APPLICATION

[0001] This application is a continuation in part of, and claims priority under 35 U.S.C. §120 from, nonprovisional U.S. patent application serial number 10/331,037 entitled "Sigma-Delta Analog-to-Digital Converter With Reduced Quantization Noise," filed on December 27, 2002, the subject matter of which is incorporated herein by reference.

is now a U.S. Patent 6,839,010

TECHNICAL FIELD

[0002] The present invention relates to analog-to-digital converters, and more specifically to using a variable low-pass filter to reduce noise in an analog-to-digital converter.

BACKGROUND

[0003] Figure 1 (prior art) is a simplified schematic block diagram of a conventional sigma-delta converter (SD converter) 10. SD converter 10 includes a sigma-delta modulator (SD modulator) portion 11 and a digital filter 12. SD modulator portion 11 is a first-order modulator and includes a summing amplifier 13, an integrator 14, a clocked comparator 15, and a switching device 16.

[0004] SD modulator portion 11 operates in cycles as determined by a clock signal of frequency kf_s that clocks